General description

BTDM001T28b2 is a low power multi-mode connectivity radio IP compliant with version 5 of the Bluetooth core specification. It supports Bluetooth BR/EDR, LE 1 Mb/s and 2 Mb/s and Bluetooth long range 500 kb/s and 125 kb/s. Additionally, BTDM001T28b2 supports IEEE802.15.4-2015 ZigBee in the 2.45 GHz ISM band. It is a complete radio + modem (PHY) designed for manufacturing in the TSMC 28 nm HPC process.

BTDM001T28b2 performs the full transceiver function from antenna to data bits. The analog radio part consists of a low-IF receiver with limited selectivity, a zero-IF IQ upmixer with linear power amplifier for EDR transmission, and a directly-modulated AD-PLL with saturated power amplifier for GFSK and OQPSK transmission. Full channel selectivity, AGC control, correction of carrier frequency offset, clock and frame synchronization and bit detection are performed in the digital part of the receiver. Mapping of data bits onto transmit symbols and pulse shaping are performed in the digital part of the transitter.The digital part of the

The receiver's AGC algorithm provides fast gain adaptation, low noise, and high dynamic range. It combines good sensitivity and C/I performance with excellent blocker performance, in excess of the standards' requirements.

BTDM001T28b2 has a single RF interface pin for shared TX output and RX input. It requires a single external capacitor for matching to 50 Ω. The TX/RX switch is integrated.

An all-digital synthesizer generates the local-oscillator signals for the transceiver, allowing fast frequency hopping while maintaining good phase noise performance. The synthesizer accepts reference frequencies between 13 MHz and 52 MHz.

The IP is designed to be self-contained. It includes a crystal oscillator circuit with integrated, tunable load capacitors for frequency reference and a one-pin crystal oscillator for timing reference (sleep clock). Thanks to a modular set up, these circuits can be carved out when they are not required, for instance when a reference frequency of sufficient quality is already present in an SoC.

On the baseband side, the unidirectional data interfaces connect to the baseband processor using a simple handshake mechanism. To ease SoC integration, the Catena connectivity IP ensures correct symbol timing.

Control is executed using a command/response/ notification mechanism. Firmware on an embedded controller decodes commands and generates responses and notifications. It also performs start-up and shut-down sequencing, executes calibration routines, and carries out general low-level radio control.

Frequency planning, supply structure and interference rejection have all been chosen to maximize co-existence performance, both as a victim and as an aggressor. This eases the integration of this IP into SoC that can contain multiple wireless connectivity IPs.

Features

General

- Compliant to Bluetooth core specification 5
- Supports BR, EDR 2 Mb/s and 3 Mb/s, LE 1 Mb/s and 2 Mb/s and LE long range 125 kb/s and 500 kb/s
- Supports 802.15.4-2015 in the 2.45 GHz ISM band for ZigBee
- Contains digital modem for all supported modulation formats
- Low power consumption
- Low-cost BoM
- Optimized frequency plan for on-chip co-existence
- Excellent blocking performance, exceeding standards requirements
- Single-pin, single-ended RF interface
- Simple matching to 50 Ω using a single capacitor
- Efficient PA delivering up to +8 dBm (Bluetooth EDR)
- Reference crystal oscillator (13MHz – 52 MHz) with integrated tunable load capacitors
- LPO crystal oscillator (32.768 kHz) for sleep clock
- Simple control through API
- Embedded controller for API command decoding and response/notification generation, start-up and shut-down sequencing, calibration routines and general low-level radio control

Key specifications

- 1.35 V analog supplies with integrated regulators
- 1.35 V PA supply for EDR mode
- 0.90 V digital supply
- Temperature range -40 - +125 °C (junction) (range for ambient dependent on package)
- Sensitivity
  - BR -95 dBm
  - EDR (2 Mb/s) -93 dBm
  - EDR (3 Mb/s) -86 dBm
  - LE (1 Mb/s) -98.5 dBm
  - LE (2 Mb/s) -95.5 dBm
  - LE (500 kb/s) -101 dBm
  - LE (125 kb/s) -103 dBm
  - 802.15.4 (250 kb/s) -100 dBm
- P_{out} +8 dBm (EDR), 14 dB control range
- Peak active current consumption (full IP)
  - RX mode (all modes)
    - 7.5 mA @ 1.35 V (VDDA)
    - 3 mA @ 0.9 V (VDDD)
  - TX mode:
    - 14 mA @ 1.35 V (+3 dBm, BR/LE/15.4)
    - 42 mA @ 1.35 V (+10 dBm, EDR)
    - 1.5 mA @ 0.9 V (VDDD, all modes)

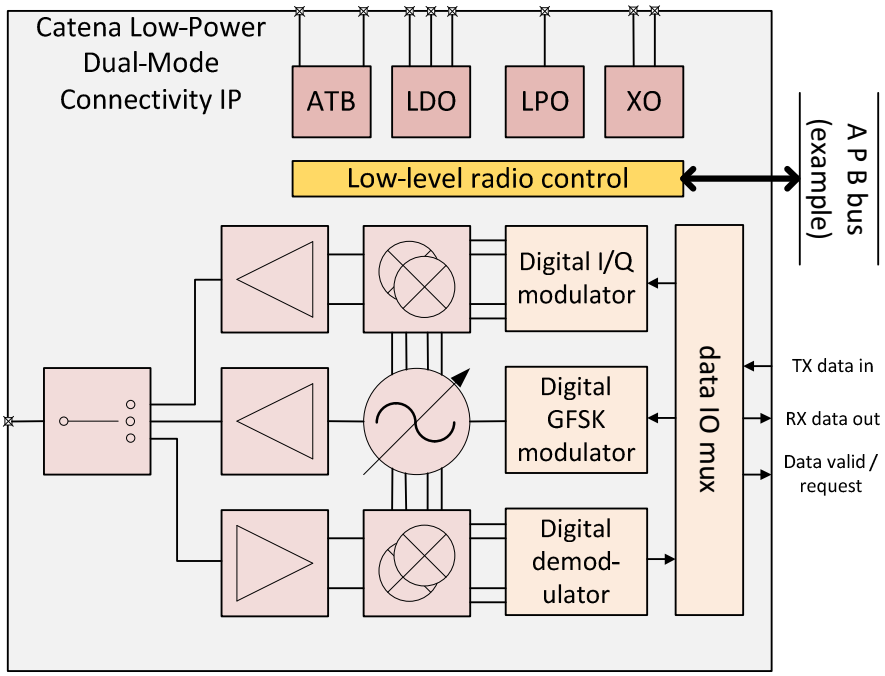

Figure 1.1 Overall block diagram

1. REFERENCE APPLICATION DIAGRAM

A typical application diagram for the Catena Connectivity IP is shown in Figure 1.1.

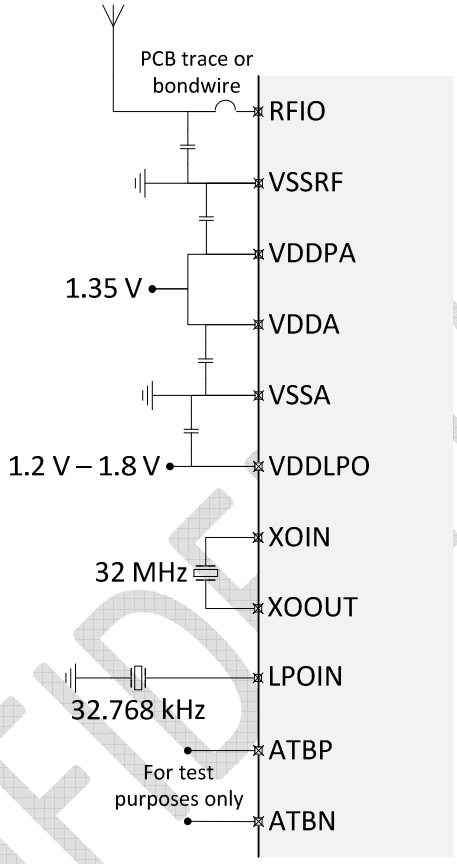

Figure 1.1 Application diagram

2. CONTACT

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