IP Specification – Short Form
WF001T28a1
1x1 concurrent dual-band 802.11ac transceiver IP

General description

WF001T28a1 is a 1x1 concurrent dual-band IEEE802.11ac transceiver IP compliant with the IEEE 802.11a/b/g/n/ac standards. It is a complete front-end optimized for high-performance WiFi applications, designed for manufacturing in the TSMC 28nm HPC process.

The WF001T28a1 IP's architecture uses direct conversion in both transmit and receive modes. Programmable analog channel filtering supports modulation bandwidths up to 80 MHz. Integrated power amplifiers and transmit/receive switches minimize application effort, board space, and BoM cost.

The WF001T28a1 IP interfaces with a customer's digital baseband processing unit. When both are integrated on the same SoC, the WF001T28a1 IP communicates with the baseband processor over an industry-standard on-chip parallel interface. Both receive and transmit paths include autonomous DC offset and IQ mismatch calibration. An internal frequency tuning loop calibrates the analog baseband filters for modulation bandwidths up to 80 MHz. The AGC algorithm, located in the digital baseband, sets the gain of the receive chains.

Frequency planning of the LO generation ensures that there is no mutual interaction between the RF and VCO signals. This avoids frequency pulling and generation of spurious output signals and spurious responses during concurrent dual-band operation.

The WF001T28a1 IP includes an internal crystal oscillator that generates the system reference frequency for the RF frequency synthesizers. Fractional-*N* synthesizers generate the local oscillator signals for the transceivers in the 5 GHz and 2.4 GHz bands, allowing concurrent dual-band operation. The WF001T28a1 IP contains a clock PLL that generates low-jitter clocks for the Rx ADCs and Tx DACs, as well as the clocks for the digital baseband. The crystal oscillator can be used as a buffer for an externally generated frequency reference signal.

A general-purpose ADC is included for customer applications, for instance to measure external sensors. A built-in temperature sensor provides temperature measurements.

Features

General

- Dual-band transceiver IP supporting IEEE802.11a/n/ac and IEEE802.11b/g/n
- Integrated linear Power Amplifiers
- Reduced bias current with reduced output power, optimizing bias conditions for different use cases
- Integrated receive/transmit switches
- Integrated analog channel filters with switchable bandwidth
- Easy-to-use calibration routines and simple interface to digital baseband
- Fractional-*N* synthesizers with fine tuning resolution and integrated loop filters
- Clock PLL generating clocks for ADCs/DACs and digital base band
- Integrated crystal oscillator for RF reference clock
- General-purpose ADC for measurement and calibration

Key specifications

- 1.5 V analog supply VDDA with integrated regulators
- 2.7 V analog supply VDDPA for power amplifiers
- 2.7 V analog supply VDDH for ADCs/DACs
- 0.9 V digital supply VDD (from SoC)
- Supported frequency bands:
  - 2.412 GHz - 2.484 GHz
  - 4.920 GHz - 5.825 GHz
- Supply current
  - Receive mode:
    From VDDA: 60 mA (low band)
    67 mA (high band)
    From VDDH: 12 mA
  - Transmit mode at P_{out} = +16 dBm (low band):
    From VDDA: 55 mA
    From VDDPA: 220 mA (No DPD)
    From VDDH: 4mA
  - Transmit mode at P_{out} = +14.5 dBm (high band):
    From VDDA: 62 mA
    From VDDPA: 280 mA
    From VDDH: 4mA
- Receive mode:
  - 20/40/80 MHz channel bandwidth
  - 4.5 dB noise figure (low band)
  - 5.5 dB noise figure (high band)
  - 63 dB gain control range
- Transmit mode:
  - 20/40/80 MHz channel bandwidth
  - +16.0 dBm output power low band (MCS-6)
  - +14.5 dBm output power high band (MCS-9)
  - 36 dB gain control

- RF reference oscillator
  - Frequency 40 MHz
- General-purpose ADC
  - Resolution 11 bits
  - Conversion time 1.2 µs

- IP core area
  - Analog hard macro (incl. ADCs/DACs) 4.3 mm^2
  - Digital soft IP (P&R dependent) 0.6 mm^2
  - Memories 8 k x 48 (1x)
    4 k x 16 (2x)
    512 x 16 (2x)

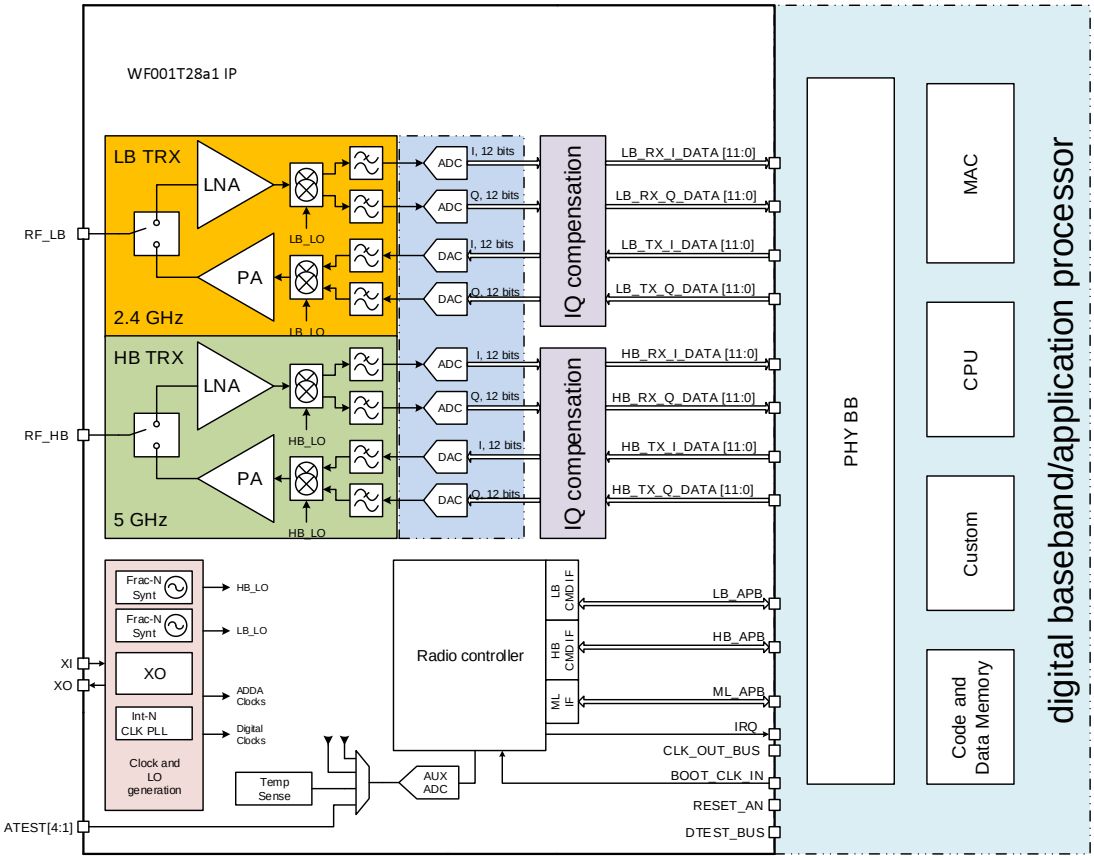

Figure 1.1 Block diagram of WF001T28a1 IP: concurrent-dual band IEEE802.11a/b/g/n/ac transceiver. The digital baseband and application processor are not included in the WF001T28a1 IP. The inclusion of these blocks is to illustrate a possible SoC implementation.

1 APPLICATION EXAMPLES

1.1 Application Using a Single Dual-Band Antenna

Figure 1.1 below shows, an application example using a single dual band antenna. The antenna is connected to the WF001T28a1 IP via a monolithic diplexer filter. This minimizes the required number of antenna matching components.

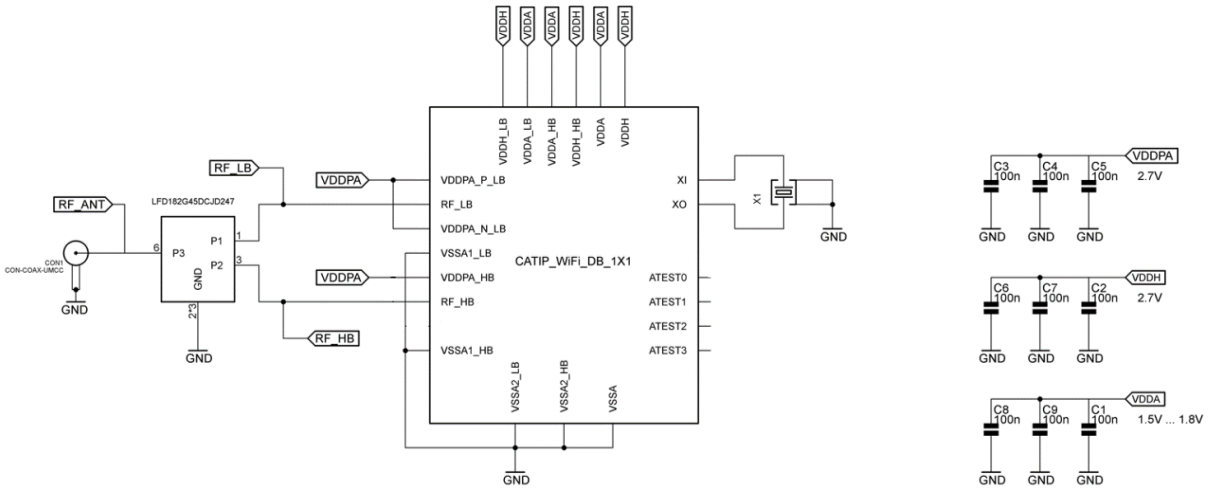

Figure 1.1 Application with single dual-band antenna and bandpass diplexer

1.2 Application Using Two Single-Band Antennas

In Figure 1.2 below, an application example is given where two separate single-band antennas are used. The antennas are connected to the WF001T28a1 IP via two separate monolithic filters.

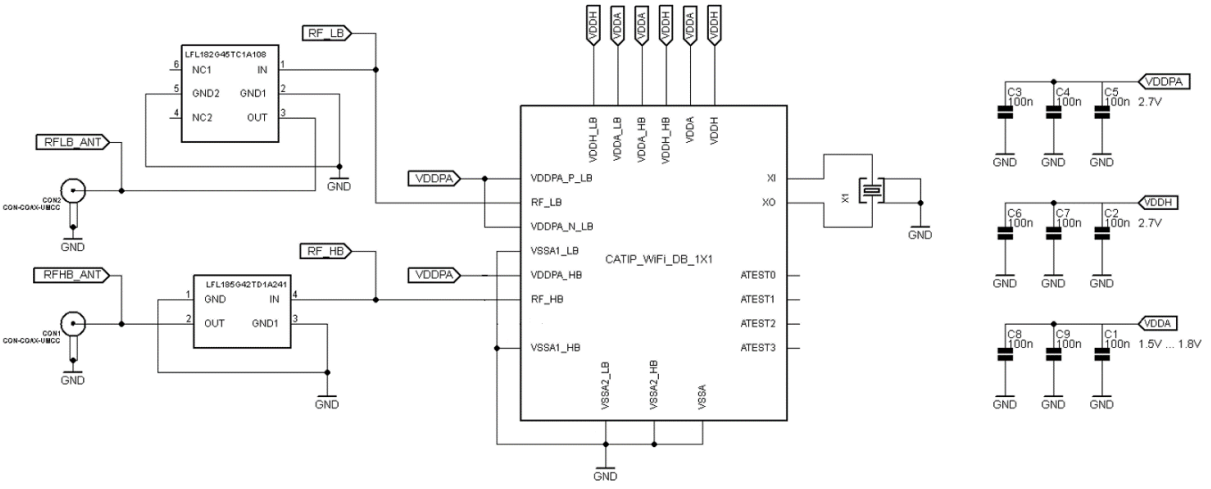

Figure 1.2 Application with two single-band antennas and band-specific low pass filters

2 CONTACT

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